AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) An amplitude limiting circuit for limiting an amplitude of a signal input to a power amplifier, comprising:

an amplitude converter which calculates an amplitude value of an input signal;

a determination unit which detects, as a detection interval, an interval in which the amplitude value exceeds a threshold, on ~~the~~a basis of a preset threshold and the amplitude value of the input signal;

a peak detector which detects, in the detection interval, a peak time when a maximum amplitude value appears and ~~an~~said maximum amplitude value at the peak time as a peak value;

a window filter which generates a window function for limiting the amplitude value to a value not more than the threshold by using the peak value output from said peak detector;

a delay circuit which delays the input signal such that the peak time output from said peak detector coincides with a time when the window function output from said window filter exhibits a minimum value; and

a multiplier which multiplies an output signal from said delay circuit by the window function.

2. (Original) A circuit according to claim 1, wherein said determination unit comprises

an amplitude comparing section which compares the preset threshold with the amplitude value of the input signal, and

an interval detecting section which detects an interval in which the amplitude value

exceeds the threshold.

3. (Currently Amended) A circuit according to claim 1, wherein

said ~~window filter outputs a~~ window function ~~which~~ exhibits a value of 1 before and after a preset correction interval longer than the detection interval and makes a value at ~~the~~a center of the correction interval proportional to ~~the~~a reciprocal of the peak value, and

said delay circuit delays the input signal such that the peak time coincides with the center of the correction interval.

4. (Currently Amended) A circuit according to claim 3, wherein said ~~window filter outputs a~~ window function ~~exhibiting~~exhibits a value which is 1 until the peak value and becomes not more than a value (threshold/peak value) at the center of the correction interval after the peak time.

5. (Original) A circuit according to claim 3, wherein

letting threshold/peak value A, $a = (1 - A)/2$, and τ be a value 1/2 a preset correction interval, said window filter outputs a window function w(t) represented by

$$w(t) = \begin{cases} 1 - a(1 - \cos(\pi t/\tau)) & (0 < t < 2\tau) \\ 1 & (t < 0, 2\tau < t) \end{cases}$$

and

said delay circuit delays the input signal by the time τ.

6. (Original) A circuit according to claim 1, further comprising a threshold input section which inputs a threshold to said determination unit.

7. (Canceled)

8. (Original) ~~An apparatus according to claim 7,~~ A CDMA communication apparatus comprising:

a plurality of filters which pass predetermined band components containing input signals;

a plurality of first frequency converters which convert the signals passing through said filters into signals with different frequencies for the respective channels;

a carrier combining unit which combines the output signals from said first frequency converters;

an amplitude limiting circuit which limits an amplitude of an output signal from said carrier combining unit, said amplitude limiting circuit comprising:

~~wherein~~

~~said amplitude limiting circuit comprises~~

an amplitude converter which calculates an amplitude value of an input signal,

a determination unit which detects, as a detection interval, an interval in which the amplitude value exceeds a threshold, on ~~the~~a basis of a preset threshold and the amplitude value of the input signal,

a peak detector which detects, in the detection interval, a peak time when a maximum amplitude value appears and an amplitude value at the peak time as a peak value,

a window filter which generates a window function for limiting the amplitude value to a value not more than the threshold by using the peak value output from said peak detector,

a delay circuit which delays the input signal such that the peak time output from said peak detector coincides with a time when the window function output from said window filter exhibits a minimum value, and

a multiplier which multiplies an output signal from said delay circuit by the window ~~function.~~function;

a D/A converter which converts an output signal from said amplitude limiting circuit into an analog signal;

a second frequency converter which converts the analog signal into an RF signal; and

a transmission power amplifier which amplifies the RF signal to power necessary for a transmission, and wherein

said delay circuit delays said input signal by a lapse time τ, where τ comprises a value set in advance to half a value corresponding to a time longer than an interval in which said input signal exceeds said threshold.

9. (New) A circuit according to claim 1, wherein said input signal comprises an in phase component I and a quadrature component Q, and said amplitude value of said input signal comprises $(I^2 + Q^2)^{1/2}$.

10. (New) An apparatus according to claim 8, wherein τ further comprises a value between 10 and 20 times a chip period used, where said chip period is a reciprocal of a

spreading frequency used in said CDMA communication apparatus.

11. (New) An apparatus according to claim 10, wherein said window function comprises w(t) represented by

$$w(t) = \begin{cases} 1 - a(1 - \cos(\pi t/\tau)) & (0 < t < 2\tau) \\ 1 & (t < 0, 2\tau < t), \end{cases}$$

and

said delay circuit delays the input signal by a time τ.